AMENDMENTS TO THE CLAIMS

Listing of claims.

1-57 (Cancelled).

58. (New) A semiconductor memory device comprising:

a semiconductor substrate having a first conductivity type and supplied with a ground potential;

a first well formed on said semiconductor substrate, having the first conductivity type and electrically connected to said semiconductor substrate;

a second well formed on said semiconductor substrate, having the first conductivity type and electrically connected to said semiconductor substrate;

a boosted low level potential applying circuit for applying a boosted low level potential higher than a low level potential of a word line;

a memory array including a memory transistor having a second conductivity type and formed on said first well, a source/drain of the memory transistor being connected to a bit line to which the boosted low level potential is applied, and a gate of the memory transistor being coupled to the word line; and

a peripheral circuit including a peripheral transistor having the second conductivity type and formed on said second well, a source of the peripheral transistor being coupled to ground.